IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. – 3. (Canceled)

4. (Withdrawn) A semiconductor integrated circuit device according to claim 1, wherein each of said plurality of first connection holes is spaced from each other so that a pitch between the adjacent first connection holes is greater than a minimum pitch between connection holes of the circuit.

5. (Withdrawn) A semiconductor integrated circuit device according to claim 4, wherein the pitch between said adjacent first connection holes is two times and more of the minimum pitch between the connection holes of said circuit.

6. (Withdrawn) A semiconductor integrated circuit device according to claim 5, wherein the pitch between said adjacent first connection holes is three times and more of the minimum pitch between the connection holes of said circuit.

7. (Withdrawn) A semiconductor integrated circuit device according to claim 6, wherein the pitch between said adjacent first connection holes is four times and more of the minimum pitch between the connection holes of said circuit.

8. (Withdrawn) A semiconductor integrated circuit device comprising: a semiconductor substrate of a first conductivity type; a zener diode comprised of a first semiconductor region of a second conductivity type formed in a primary face of said semiconductor substrate, and a second semiconductor region of said first conductivity type formed in said semiconductor substrate at a bottom portion of said first semiconductor region and being smaller than said first semiconductor region in an area surrounding a planar pattern thereof,

wherein a plurality of first connection holes for electrically connecting said first semiconductor region and a wire to each other are arranged in a region being outside a junction formed between said first semiconductor region and said second semiconductor region, and wherein each of said plurality of first connection holes is spaced apart from others of said connection holes so that a pitch between the adjacent first connection holes is greater than a maximum pitch between connection holes of the circuit.

9. (Withdrawn) A semiconductor integrated circuit device according to claim 8, wherein a junction depth of said first semiconductor region in a region in which said first and second semiconductor regions form a junction is shallower than that of said semiconductor region in a region in which said semiconductor substrate and said first semiconductor region form a junction.

10. (Withdrawn) A semiconductor integrated circuit device according to claim 8, wherein each of said plurality of first connection holes is equal to and

smaller than a connection hole arranged with a minimum pitch of the circuit in diameter.

11. (Withdrawn) A semiconductor integrated circuit device comprising:

a plurality of first connection holes for electrically connecting a first wire and a first semiconductor region formed in a first region of a primary face of a semiconductor substrate, to each other therethrough; and

a plurality of second connection holes for electrically connection a second wire and a second semiconductor region formed in a second region of the primary face of the semiconductor substrate, to each other therethrough, wherein each of said plurality of first connection holes is spaced from others of said first connection holes so that a pitch between the adjacent first connection holes is greater than a minimum pitch between connection holes of the circuit, and wherein each of said plurality of second connection holes is spaced from others of said second connection holes so that a pitch between adjacent second connection holes substantially equal to the minimum pitch of the connection holes of the circuit.

12. – 14. (Canceled)

15. (Withdrawn) A semiconductor integrated circuit device comprising:

a first semiconductor region of a first conductivity type formed in a primary face of a semiconductor substrate;

a second semiconductor region of said first conductivity type formed on said semiconductor substrate at an upper part of said first semiconductor region, said

second semiconductor region having a higher impurity concentration than said first semiconductor region;

a third semiconductor region of a second conductivity type formed in said semiconductor substrate at upper parts of said first and second semiconductor regions;

a first insulation film formed on said primary face of said semiconductor substrate;

a first connection hole comprised of a plurality of connection holes formed in said first insulation film at said upper part of said first semiconductor region; and

a second connection hole comprised of a plurality of connection holes formed in said first insulation film at said upper part of said third semiconductor region, wherein said second connection hole is formed in an upper part of a region in which said first semiconductor region and said third semiconductor region from a junction.

16. (Withdrawn) A semiconductor integrated circuit device according to claim 15, wherein a first electrically conductive connection body of said first conductivity type and a second electrically conductive connection body of said second conductivity type are provided inside said first and second connection holes, respectively, and wherein a first wire electrically connected to said first semiconductor region via said first electrically conductive connection body, and a second wire electrically connected to said third semiconductor region via said second electrically connecting connection body are formed at said upper part of said first insulation film.

17. (Withdrawn) A semiconductor integrated circuit device according to claim 16, wherein said first semiconductor region is comprised of a fourth semiconductor region of said first conductivity type, and a fifth semiconductor region electrically connected to said first electrically conductive connecting body via said fourth semiconductor region, wherein an impurity concentration of said fifth semiconductor region is lower than an impurity concentration of said fourth semiconductor region.

18. (Withdrawn) A semiconductor integrated circuit device according to claim 15, wherein said first and second connection holes are formed by using a photo-resist film as a mask and by dry etching said first insulation film.

19. (Withdrawn) A semiconductor integrated circuit device comprising:

a first semiconductor region formed in the primary face of a semiconductor substrate;

a second semiconductor region of a first conductivity type formed on said semiconductor substrate at an upper part of said first semiconductor region;

a third semiconductor region of a second conductivity type formed on said semiconductor substrate at upper parts of said first and second semiconductor regions;

a first insulation film formed on said primary face of said semiconductor substrate;

a first connection hole comprised of a plurality of connection holes formed on said first insulation film at said upper part of said first semiconductor substrate; and

a second connection hole comprised of a plurality of connection holes formed on said first insulation film at an upper part of said third semiconductor region, wherein a minimum pitch between adjacent connection holes of said second connection hole is greater than a minimum pitch between adjacent connection holes of said first connection hole.

20. (Withdrawn) A semiconductor integrated circuit device according to claim 19, wherein said first semiconductor region is a semiconductor region of said second conductivity type and is lower than said second semiconductor region in a impurity concentration.

21. (Withdrawn) A semiconductor integrated circuit device according to claim 19, wherein said first semiconductor region is a semiconductor region of said second conductivity type that forms a collector region of a bipolar transistor, said second semiconductor region is a semiconductor region of said first conductivity type that forms a base region of said bipolar transistor, and said third semiconductor region is a semiconductor region of said second conductivity type that forms an emitter region of said bipolar transistor.

22. (Canceled)

23. (Withdrawn) A semiconductor integrated circuit device according to claim 22, wherein each of said plurality of first connection holes is spaced from

others so that a pitch between adjacent first connection holes is greater than a ~~minimum pitch between connection holes of the circuit.~~

24. – 38. (Canceled)

39. (Currently Amended) A semiconductor integrated circuit device comprising:

a semiconductor substrate of a second conductivity type;

a plurality of first well regions of a first conductivity type formed in said semiconductor substrate;

at least a first zener diode and a second zener diode connected in series and comprised of

(i) ~~a~~one of said first well ~~region of a first conductivity type formed in said semiconductor substrate~~regions,

(ii) at least two spaced-apart, second well regions of said second conductivity type formed in said one first well region, each of said second well regions being associated with different ones of said zener diodes,

(iii) first semiconductor regions of said first conductivity type formed in said second well regions, respectively, and

(iv) second semiconductor regions of said second conductivity type formed at a bottom portion of said first semiconductor regions, respectively, and each being smaller in area, defined by a planar pattern thereof, than said first semiconductor region corresponding thereto;

an insulation film formed over a primary face of said semiconductor substrate;

a plurality of first connection holes for providing electrical connections therethrough to said first semiconductor regions and a plurality of second connection holes for providing electrical connections therethrough to said second well regions being formed in said insulation film; and

a wiring formed over said insulation film and connecting said first connection holes which are for electrical connection to the first semiconductor region of said first zener diode and said second connection holes which are for electrical connection to the second well region of said second zener diode,

wherein said first connection holes associated with said first zener diode are arranged in a region located outside a junction formed between said first semiconductor region and said second semiconductor region of said first zener diode,

wherein a first PN junction is formed between ones of said first semiconductor regions and corresponding ones of said second semiconductor regions and functions as a diode device, and a second PN junction is formed between said one first well region and said second well regions, respectively, and has a breakdown voltage greater than that of said first PN junction, ~~and~~

wherein a junction depth of each of said first semiconductor regions in a region in which said first PN junction is formed is shallower than that of each of said first semiconductor regions in a region in which said first PN junction is not formed, and

wherein a MISFET is formed in another one of said first well regions.

40. (Previously Presented) A semiconductor integrated circuit device ~~according to claim 39, wherein said second semiconductor regions are arranged~~ substantially at a center location of said first semiconductor regions, respectively, and said plurality of first connection holes are arranged at a periphery of said first semiconductor regions, respectively.

41. (Previously Presented) A semiconductor integrated circuit device according to claim 40, wherein said second semiconductor regions have an impurity concentration higher than that of said second well regions.

42. (Previously Presented) A semiconductor integrated circuit device according to claim 39, wherein said second semiconductor regions have an impurity concentration higher than that of said second well regions.

43. (Currently Amended) A semiconductor integrated circuit device according to claim 39, wherein said first conductivity type is ~~taken from one of~~ an n-type ~~and a p-type conductivities~~conductivity, and said second conductivity type is ~~the other of said n-type and~~ a p-type ~~conductivities~~conductivity.

44. (Currently Amended) A semiconductor integrated circuit device comprising:

a semiconductor substrate of a second conductivity type;

a plurality of first impurity ~~region~~regions of a first conductivity type formed in said semiconductor substrate,

a plurality of diodes connected in series, at least a first diode and a second diode of said plurality of diodes include, respectively,

(i) a second impurity region of a second conductivity type formed in one of said first impurity ~~region~~regions,

(ii) a third impurity region of a first conductivity type formed in said second impurity region, and

(iii) a fourth impurity region of a second conductivity type formed in said second impurity region under said third impurity region,

wherein said one first impurity region is common to said at least first and second series-connected diodes;

an insulation film formed over a primary face of said semiconductor substrate;

first plugs for electrically connecting therethrough to said third impurity region and second plugs for electrically connecting therethrough to said second impurity region of said first and second diodes, respectively, said first and second plugs being formed in said insulation film; and

a ~~conductive layer~~first wire formed over said insulation film ~~and~~, connected via ones of said first plugs to said third impurity region of said first diode and connected via ones of said second plugs to said second impurity region of said second diode,

a second wire formed over said insulation film and connected via ones of said second plugs to said second impurity region of said first diode,

a third wire formed over said insulation film and connected via ones of said first plugs to said third impurity region of said second diode,

wherein said third impurity region has a first portion and a second portion, said first portion is that in which a first PN junction is formed between said third and fourth impurity ~~region~~regions and said second portion is that below which said fourth impurity region is not formed,

wherein a junction depth of said first portion is shallower than that of said second portion, ~~and~~

wherein said second portion is formed outside said first portion, and said first plugs are formed over said second portion of said third impurity region, and

wherein said first, second and third wires are formed at a same layer.

45. (Previously Presented) A semiconductor integrated circuit device according to claim 44, wherein at least said first and second diodes are zener diodes, respectively.

46. (Previously Presented) A semiconductor integrated circuit device according to claim 44, wherein said second portion is formed in a periphery of said first portion so as to surround said first portion, and said first plugs are arranged over said second portion so as to surround said first portion.

47. (Previously Presented) A semiconductor integrated circuit device according to claim 46, wherein said fourth impurity region has an impurity concentration higher than that of said second impurity region.

48. (Currently Amended) A semiconductor integrated circuit device ~~according to claim [[47]]~~46, ~~wherein said first conductivity type is taken from one of~~ an n-type ~~and a p-type conductivities~~conductivity, and said second conductivity type is ~~the other of said n-type and~~a p-type ~~conductivities~~conductivity.

49. (Currently Amended) A semiconductor integrated circuit device according to claim 46, wherein a breakdown voltage of a second PN junction formed between said one first impurity region and second impurity ~~regions~~region is greater than that of said first PN junction.

50. (Previously Presented) A semiconductor integrated circuit device according to claim 44, wherein said fourth impurity region has an impurity concentration higher than that of said second impurity region.

51. (Currently Amended) A semiconductor integrated circuit device according to claim 50, wherein a breakdown voltage of a second PN junction formed between said one first impurity region and second impurity ~~regions~~region is greater than that of said first PN junction.

52. (Previously Presented) A semiconductor integrated circuit device according to claim 44, wherein a breakdown voltage of a second PN junction formed between said first and second impurity regions is greater than that of said first PN junction.

53. (Currently Amended) A semiconductor integrated circuit device comprising:

a first diode and a second diode connected in series and commonly formed in one of a plurality of first well ~~region~~regions of a first conductivity type, said one first well region being formed on a semiconductor substrate, and said first diode and said second diode, respectively, comprising

(i) a second well region of a second conductivity type formed in said one first well region,

(ii) a first semiconductor region of a first conductivity type formed in said second well region, and

(iii) a second semiconductor region of a second conductivity type, said second semiconductor region being formed in said second well region and under said first semiconductor region;

an insulation film formed over a primary face of said semiconductor substrate;

a plurality of first connection holes for providing electrical connections therethrough to said one first semiconductor region and a plurality of second connection holes for providing electrical connections therethrough to said second well region being formed in said insulation film; and

a ~~wiring~~first wire formed on said insulation film and connecting said first connection holes which are for electrical connection to said first semiconductor region of said first diode and said second connection holes which are for electrical connection to said second well region of said second diode,

a second wire formed over said insulation film and connected via ones of said second connection holes to said second well region of said first diode,

a third wire formed over said insulation film and connected via ones of said first connection holes to said first semiconductor region of said second diode,

wherein said second semiconductor region has an impurity concentration higher than that of said second well region,

wherein said first semiconductor region has a first portion and a second portion, said first portion is that below which said second semiconductor region is formed and said second portion is that below which said second semiconductor region is not formed,

wherein a first PN junction is formed between said second semiconductor region and said first semiconductor region at said first portion and constitutes a zener diode,

wherein a junction depth of said first portion is shallower than that of said second portion, said second portion is formed in a periphery of said first portion so as to surround said first portion,

wherein said plurality of first connection holes are arranged over said second portion so as to surround said first portion, and

wherein a second PN junction is formed between said one first well region and said second well region and has a breakdown voltage greater than that of said first PN junction,

wherein said first, second and third wires are formed from a same layer, and

wherein a MISFET is formed in another one of said first well regions.

54. (Previously Presented) A semiconductor integrated circuit device according to claim 53, wherein said first and second conductivity types are a p-type conductivity and an n-type conductivity, respectively.

55. (Previously Presented) A semiconductor integrated circuit device according to claim 53, wherein said first and second conductivity types are a n-type conductivity and an p-type conductivity, respectively.

56. (New) A semiconductor integrated circuit device according to claim 39, wherein said first conductivity type is a p-type conductivity, and said second conductivity type is an n-type conductivity.

57. (New) A semiconductor integrated circuit device according to claim 44, wherein said first conductivity type is a p-type conductivity, and said second conductivity type is an n-type conductivity.

58. (New) A semiconductor integrated circuit device according to claim 44, wherein a MISFET is formed another one of said first impurity regions.